Experiment #1 – VNA Calibration

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# EEL5439C RF and Microwave Active Circuits

Prof. Dr. Kenle Chen - Section 0012

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# **Experiment Objective**

The objective of this experiment is to learn PCB fabrication, SOLT and TRL VNA calibration and to design microwave circuity using Advanced Design Systems (ADS).

# **2.0 Q&A**

1. A diagram of a circular object

   Description automatically generated with medium confidenceA diagram of a circle with numbers and symbols

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   Description automatically generatedA diagram of a circle with numbers and a blue dot

   Description automatically generatedA diagram of a graph

   Description automatically generatedYou can present S parameters using Smith Chart, X-Y graph (magnitude or phase, real or imaginary). It is your decision regarding which format to use. But the one you pick should help you explain the results clearly.

A diagram of a circle

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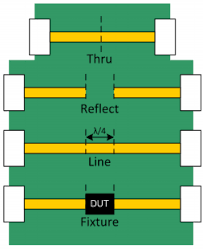
A diagram of a circle

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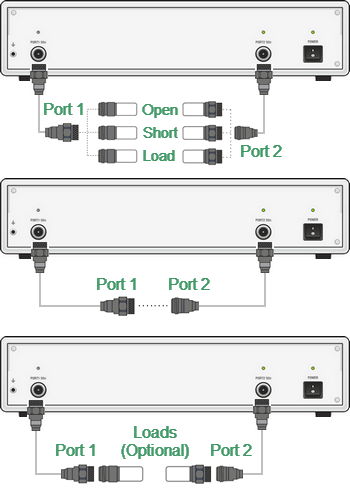
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1. Why do you use TRL instead of SOLT calibration for the measurement? Point out your reference plane for each case on the picture. Which kind of errors if you use SOLT calibration? Can you use theory to compensate the errors? How?

TRL can be used over full two-port SOLT calibration due to speed and higher accuracy of measurements. TRL requires less measurements which reduces operator error and calibration time. In addition, TRL calibration is critical for measurements where the phase measurement is important; this is because in SOLT calibration the reference plane is moved to coaxial connectors of the VNA whereas with TRL calibration the reference plane is moved all the way to DUT plane. TRL measurement is best for smaller components.



Source: [Copper Mountain](https://coppermountaintech.com/wp-content/uploads/2018/05/Design-and-Fabrication-of-a-TRL-Calibration-Kit.pdf)[1]



Source: [Copper Mountain[2]](https://coppermountaintech.com/help-s2/full-two-port-calibration.html)

In SOLT calibration, the phase measurement will offset from the true measurement due to the phase change caused by the transmission line. This error can be reduced in post-processing of data by applying the following transformation to move the reference plane forward using the following equations:

A close-up of a mathematical equation

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Source: Dr. Xun Gong, Lecture 8 – S Parameters

1. Show how you determine the TRL standard length and maximum frequency range.

The lead transmission line and reflect line should be long. The reflect line represents open load, the reason for the reflect line length of is to convert a short to an open load. The reflect line is used as reference load for DUT measurements. The frequency range is based on the LINE length, the line length can have a maximum of 30-degree shift from center frequency for reasonably accurate measurements. The LINE length can be determined using the following constraints:

Where is wave velocity, for microstrip line can be determined by .

= Reference line length

= TRL line length

1. Show the calibrated responses of the through, line, and reflect using TRL cal. Comment on your results.

See previous question for smith chart plots.

The TRL measurements represent the lumped elements components more accurately because in the SOLT measurements, the reactance of the lumped elements was shifted due to transmission line length effects. For example, the inductor when using SOLT, the inductance was measured to be ( normalized) which was equivalent to . However, when using TRL measurements, the inductance was measured to be ( normalized) which was equivalent to 3.12 a much closer value compared to SOLT measurement. It is important to note that the inductor used in the lab has tolerance and would not be exactly and lab fabrication is not extremely precise.

1. Graph the S parameters of the lumped elements using both calibration methods. Also extract the resistance, capacitance, and inductance value of each component. Please note that you need to also plot the component values versus frequency. Comment on your results.

See previous questions for S parameters plot.











1. Can you use the low-frequency capacitor for 1 GHz circuit? Why?

It depends on the specification of the design, a discrete capacitor (lumped element) can be used but it will experience higher loss due parasites compared to distributed element such as a transmission line. The loss may be acceptable for some applications and in that case, it would be possible to use a capacitor. In addition to losses, the non-ideal capacitor will experience resonance at a certain frequency due to the series inductance caused by capacitor wire leads. Self-Resonance Frequency (SRF) may pose additional design challenges.

1. Does the RF choke behave like an open at 1 GHz? You will use it for your amplifier biasing.

It depends on what was used to construct the RF choke; if the RF choke is realized with a distributed element such as microstrip line, then it will behave as an open at the center frequency and integer multiples of the center frequency. If lumped element is used for the RF choke, then the inductor will behave as open at the cut-off frequency and afterwards, however, the lumped element inductor will be more lossy than the distributed element inductor. The lumped element impedance will increase with frequency defined by this equation: .

1. Is the chip component performance good enough for 1 GHz applications?

It depends on the requirements of the design, realized lumped elements on semiconductor chips have lower quality (due to lossy substrate) and lower power handling (due to size). For lower power solutions, it would be possible to use IC components, however, if higher power is needed or higher quality factor, then a chip component would not be suitable.

1. The grounding vias will introduce parasitic inductance. How to minimize this inductance? (extra points: characterize the parasitic inductance using any full-wave simulation software such as momentum in ADS.)

There are two methods of reducing parasitic inductance of the vias, the first is changing the length of the transmission line such that it would approach the center of the smith chart, therefore matching the source to the load. Another approach is to add a series capacitor to the via which will reduce the inductance of the “vias”. Each approach has its own benefits and disadvantages, the series capacitor is simpler and does not require a change in transmission line length which could be difficult to realize, however, the lumped element will suffer from its own parasitic and introduce greater loss to the circuit. The alteration of the transmission line length would not suffer from parasitic, however, the matching will only occur at the center frequency and the effectiveness of the matching will be reduced with drifts to the frequency, the transmission line also may require a size increase of the circuit which may not be possible in small form factor devices.

## Characterization of Parasitic Inductance; Simulation by Ansys HFSS

A diagram of a square object

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Simulation Structure

|  |  |
| --- | --- |
| Structure Property | Value |
| Substrate Width | 10 mm |
| Substrate Height | 10 mm |
| Substrate Thickness | 32 mil |
| Substrate Material | Rogers 4003C |
| Microstrip line width | 70 mil ( |
| Microstrip length | 6 mil |
| Via radius | 35 mil |
| Copper Thickness | Planar Sheet |
| Copper Conductivity | Finite Conductivity, |

|  |  |
| --- | --- |
| Simulation Property | Value |
| Start Frequency | 0.5 GHz |
| Center Frequency | 1 GHz |
| Stop Frequency | 2 GHz |
| Max Pass Count | 10 |
| Max S. Delta | 0.02 |
| Sweep Type | Interpolating |
| Point Count | 1000 |

A circular graph with numbers and a red line

Description automatically generated with medium confidence

Simulation Result

The inductance value ranged from 0.0842j to 0.3445j (normalized impedance to 50 ) from 0.5 GHz to 2 GHz respectively. The equivalent inductance values can be computed using the following method:

|  |  |  |  |
| --- | --- | --- | --- |
| Frequency |  |  | Inductances () |
| 500 MHz |  |  | 1.34 |
| 1.00 GHz |  |  | 1.34 |
| 2.00 GHz |  |  | 1.37 |

# **3.0 Conclusion**

In conclusion, the experiment focused on VNA calibration, specifically exploring PCB fabrication, SOLT and TRL VNA calibration, and designing microwave circuits using Advanced Design Systems (ADS). The choice between TRL and SOLT calibration methods was addressed, with a preference for TRL due to its speed, higher accuracy, and reduced operator error. TRL calibration is particularly advantageous for applications where phase measurements are crucial, as it allows the reference plane to be moved to the DUT plane.

The experiment successfully demonstrated the calibration of through, line, and reflect responses using TRL calibration. The results indicated that TRL measurements more accurately represent lumped element components compared to SOLT measurements, where the reactance of lumped elements can be affected by transmission line length effects. For instance, the inductance of a 1.8 nH inductor was measured more accurately with TRL calibration, showing the importance of the calibration method in obtaining reliable component values.

Graphical representations of S parameters using both calibration methods were presented, and the resistance, capacitance, and inductance values of each component were extracted. The performance of components, such as low-frequency capacitors and RF chokes, was discussed in the context of their suitability for 1 GHz applications. The influence of grounding vias and methods to minimize parasitic inductance were also explored, including the use of series capacitors and adjustments in transmission line length.

A detailed simulation of parasitic inductance in grounding vias using Ansys HFSS provided insights into the frequency-dependent behavior of the vias. The simulation results indicated varying inductance values across the frequency range, emphasizing the need to carefully consider and mitigate parasitic effects in practical designs.

In summary, the experiment provided valuable hands-on experience in VNA calibration, component characterization, and the consideration of parasitic effects in microwave circuit design. The results and insights gained contribute to a better understanding of the challenges and considerations in designing and optimizing microwave circuits for specific applications.